http://embeddedandvlsidesignconference.org/

The 32nd International Conference on VLSI Design & The 18th International Conference on Embedded Systems

January 5-9, 2019, (New Delhi, National Capital Region, India)

The Go Green Conference

IMPORTANT DATES

Full paper submission:	**August 10, 2018 (hard deadline)**
Acceptance notification:	September 23, 2018
Camera ready paper:	October 7, 2018
Tutorials/Workshops:	January 5-6, 2019
Conference:	January 7-9, 2019

CALL FOR PAPERS

This joint conference is a forum for researchers and designers to present and discuss current topics in VLSI design, EDA, embedded systems, and emerging technologies. Two days of tutorials (January 5-6) will be followed by three days (January 7-9) of regular paper sessions, special sessions, and embedded tutorials. The program will also include industry sessions along with exhibits, panel discussions, design contest, and Ph.D. forum.

TOPICS OF INTEREST

Regular papers are invited in all areas of VLSI design and embedded systems, including but not limited to the following categories:

Autonomous Intelligence Smart autonomous systems, machine learning techniques, cognitive systems, artificial intelligence, machine learning for VLSI CAD, data analytics, neuromorphic and brain-inspired computing, and case studies.	**Embedded Systems** System-level design, HW/SW co-design, multi-core SoCs, embedded processor and memory design, networks-on-chip, defect-tolerant architectures, accelerators, FPGA and reconfigurable systems, parallelization, virtualization, firmware, middleware, case studies.	**Security & Privacy** Embedded systems security, hardware security, IP trust, physically unclonable functions, random number generators, fault tolerant systems and architectures, system security, side channel attacks and countermeasures	**IoT and Cyber-Physical Systems** Internet-of-Things (IoT) devices, cyber-physical systems, sensors, actuators, displays, control systems, and design for safety and certifications in airborne, health care, automotive & IoT applications
Power & Energy Low-power design, low-power systems, wireless power delivery, Power analysis and estimation, optimization and low-power design, energy-efficient design, thermal management, energy harvesting, approximate computing	**Test & Verification** Simulation, formal verification, validation at different abstraction levels, DFT, fault modelling and simulation, ATPG, BIST, fault tolerance, post-silicon validation and debug, delay test, memory test, reliability testing	**Design Automation Algorithms** Logic and behavioral synthesis, logic mapping, simulation and formal verification, layout (partitioning, placement, routing, floor planning, and compaction), post route optimizations	**RF Design** RF IP design, low-power and high-speed RFICs, RF modeling and CAD simulation, RFIC technologies, circuits, devices, fabrication, testing, reliability, and packaging; synthesis and verification, noise analysis.
Digital Design Logic and physical synthesis, place and route, clock tree design, timing and signal integrity, design for manufacturability and yield, power integrity, variation-tolerant design	**Analog Mixed Signal** Design of analog and mixed signal IPs, high-speed wired and wireless interfaces, low-power analog design, analog and mixed-signal modeling, synthesis and validation	**CMOS Technology and Devices** Deep nanoscale CMOS devices, device modelling and simulation, multi-domain simulation, device/circuit-level reliability and variability	**Emerging Technologies** Post-CMOS devices, MEMS sensors, biomedical circuits, lab-on-chip, carbon nanotubes, silicon photonics, spintronics, memristors, neuromorphic/quantum computing

THREE SPECIAL ISSUES

Highest ranked papers from regular submissions will be invited to the thematic special issues of the following journals:

- **IEEE Transactions on VLSI Systems** (on security and privacy)
- **IET Computers & Digital Techniques** (on energy-aware computing)
- **IETE Journal of Research** (on machine learning)

SUBMISSIONS

All submissions should be made electronically via the conference website http://embeddedandvlsidesignconference.org/ by **August 10, 2018**. Your manuscript should clearly state the novel ideas, results, and applications of the contribution. Paper submissions will undergo a double-blind review. Papers must be in PDF format and not exceed 6 single-spaced pages including figures and references in two-column IEEE conference paper format (10pt font). Papers exceeding the page limit or identifying the authors will be rejected without review.

BEST PAPER AWARDS

Top papers will be considered for the **Best Paper Award**, **Best Student Paper Award**, and **Honorable Mention Award**.