Title: FinFETs: Quo Vadis?

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At the 22nm technology node, the semiconductor industry started moving decisively towards FinFETs, which come in double-gate and tri-gate flavors, from bulk CMOS. This boosted performance and lowered leakage power. However, even with these advantages, the power wall still looms, dark silicon still threatens us, and process variations have not stopped giving us headaches. This talk asks where we are going with FinFETs and variants of these devices, and circuits and architectures based on this technology. We will see that the FinFET design space is much vaster than the CMOS design space. This leads to many interesting design problems at each level of the IC design hierarchy. We will ask if we have the simulation and design infrastructure ready to start addressing these problems.

***Biography**:* Niraj K. Jha received his B.Tech. degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India in 1981 and Ph.D. degree in Electrical Engineering from University of Illinois at Urbana-Champaign in 1985. He is a Professor of Electrical Engineering at Princeton University. He also serves as an Associate Director for the Princeton Andlinger Center for Energy and the Environment. He is a Fellow of IEEE and ACM. He received the Distinguished Alumnus Award from IIT, Kharagpur in 2014. He has co-authored or co-edited five books, among which are “Switching and Finite Automata Theory, 3rd ed.” and “Testing of Digital Systems” that are textbooks being used around the world. He has served as the editor-in-chief of IEEE Transactions on VLSI Systems and on the editorial boards of several other IEEE Transactions. He is an author or co-author of more than 400 papers among which are 14 award-winning papers. His research interests include FinFETs, power analysis and optimization, IC design automation, computer architecture, computer security, quantum computing, and energy-efficient buildings.