FinFETs: Quo Vadis?

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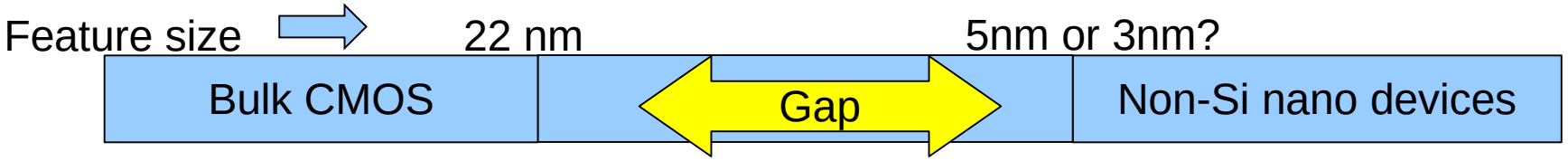
Talk Outline

- Quo Vadis FinFET devices?
- Quo Vadis FinFET standard cells and logic circuits?
- Addressing the Power Wall with FinFET variants
- Conclusions

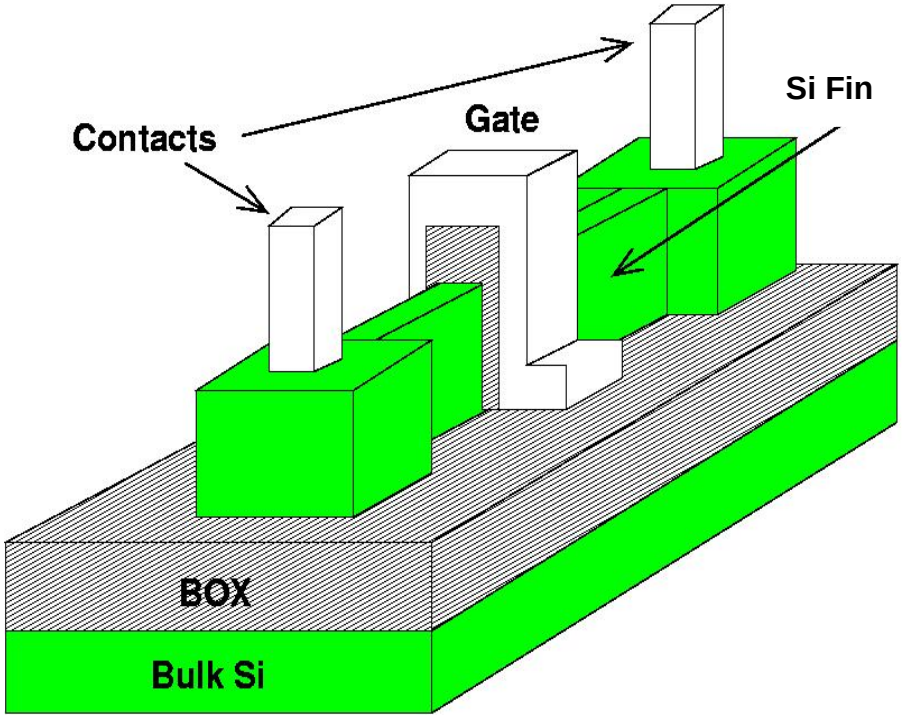
Why FinFETs?



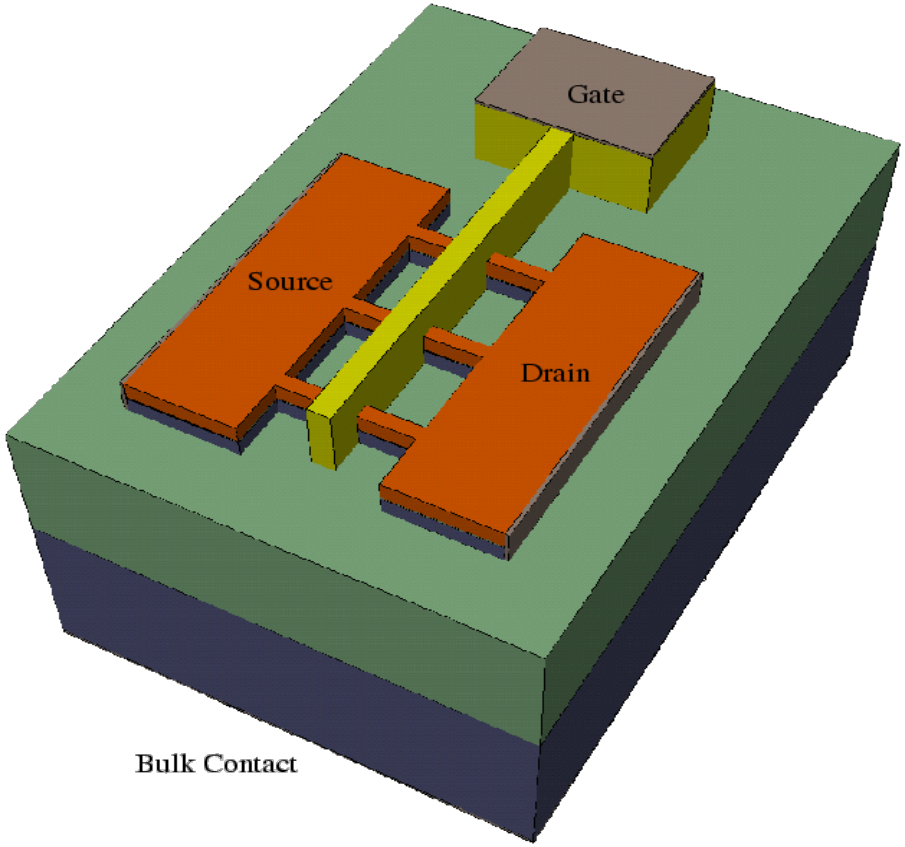
- FinFETs: extensions of CMOS
  - Manufacturing processes similar to CMOS
- Key limitations of CMOS scaling addressed through
  - Better control of channel from transistor gates
  - Reduced short-channel effects
  - Better I_{on}/I_{off}
  - Improved subthreshold slope
  - No discrete dopant fluctuations

What are FinFETs?

- Fin-type FET
  - Like a FET, but channel “turned on its edge” and made to stand up



FinFET 3-D Structure



Shorted-gate multi-fin

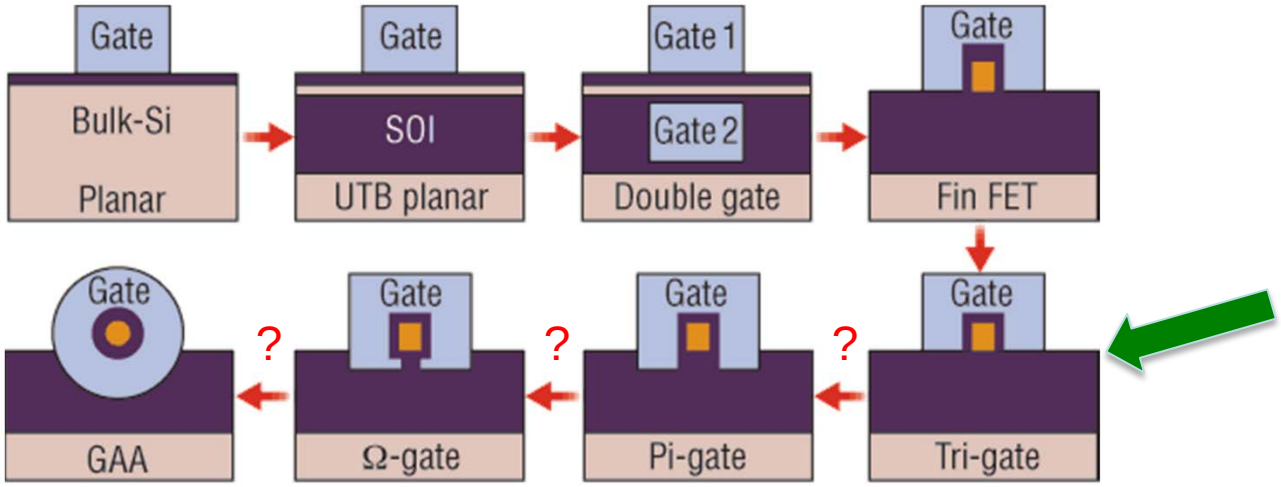
(Ananthan, 2004)

Quo Vadis FinFET Devices?

Three Challenges

- Challenge 1: how far can FinFETs be scaled?
- Challenge 2: at a given technology node, what FinFET variants are possible and which ones should be deployed?
- Challenge 3: how do you simulate the FinFET variants?

Challenge 1: FinFET Scaling



Currently, we are here

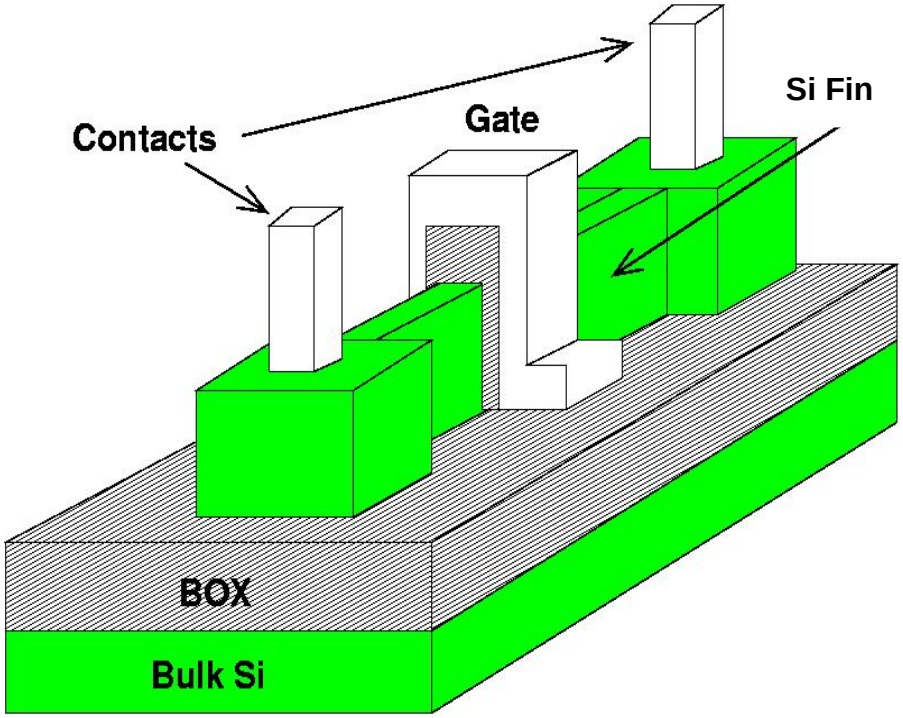
- Scaling possible till which technology node: 5nm? 3nm?
- If FinFETs can be scaled to 3nm, would alternative nano devices be economically viable for further scaling?

http://www.electroiq.com/content/eiq-2/en/articles/sst/print/volume-51/issue-5/features/nanotechnology/fully-gate-all-around-silicon-nanowire-cmos-devices.html

Challenge 2: FinFET Variants

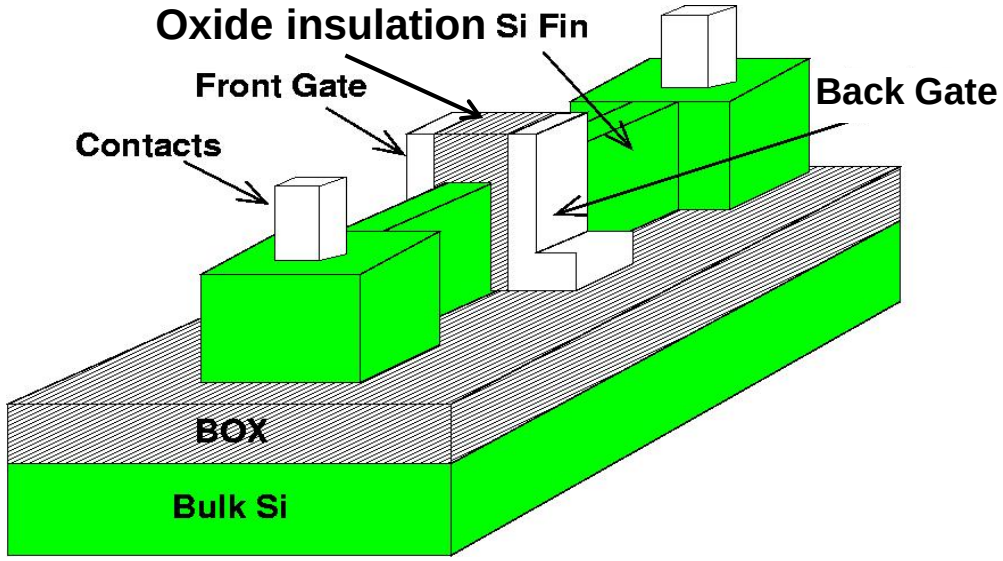
- Shorted-gate (SG)
- Independent-gate (IG)
- Asymmetric FinFETs
  - Single-parameter asymmetry
  - Multiple-parameter asymmetry

Traditional FinFET: SG



- Good I_{on}
- Not-so-good I_{off}

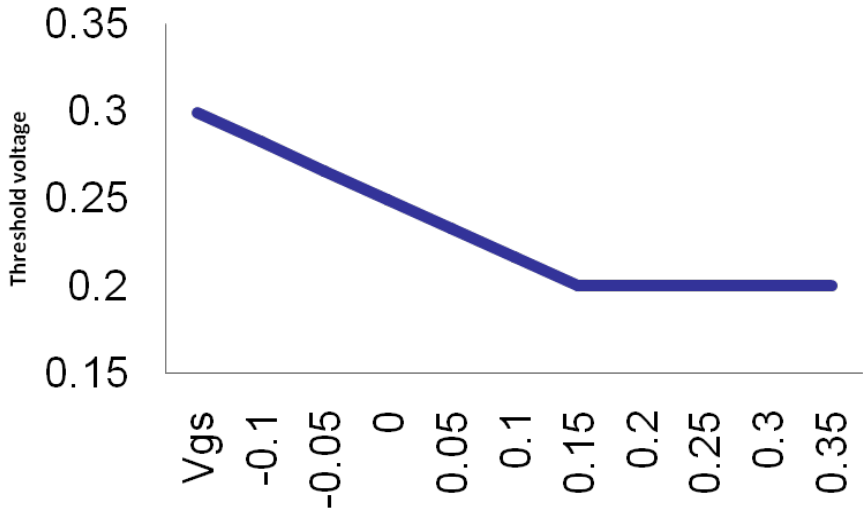
Independent-gate (IG) FinFET



- FET gates independently controllable
  - Extra process step
  - Degraded I_{on}
  - Order-of-magnitude lower I_{off}
  - Leads to novel analog and digital circuit structures

IG FinFETs: Three Operation Modes

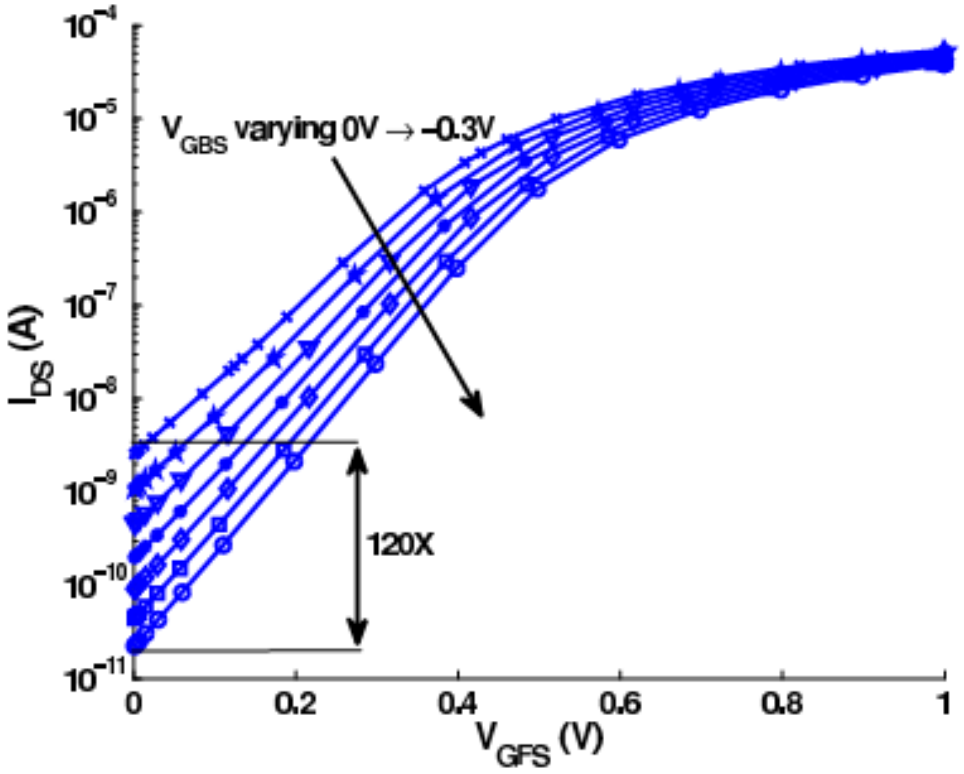
- Mode 1: Reverse/forward bias the back gate to control the V_{th} of the front gate



  - IG FinFET: V_{th} varies linearly with back-gate bias
  - Bulk CMOS: V_{th} varies as square-root of body bias
  - Runtime micro-DPM: effect leakage-delay tradeoff with a breakeven point of only five clock cycles

Back-gate Biasing Effect

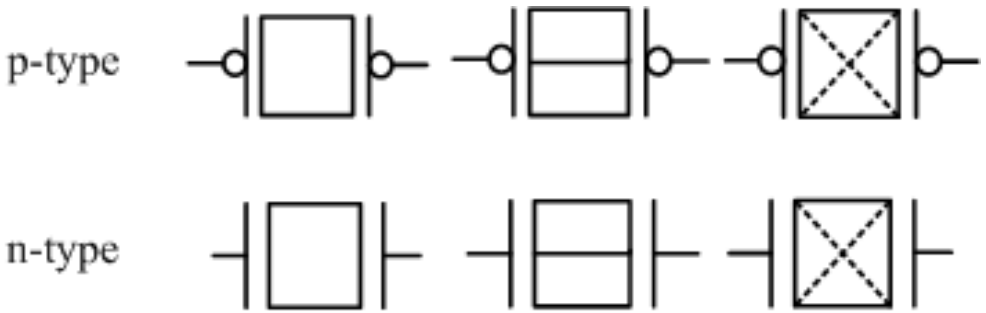
- Chosen FET device parameters yield 120X leakage reduction in IG-mode



(Bhoj-Jha, 2011)

IG FinFETs: Operation Modes (Contd.)

- Mode 2: low-V_{th} OR operation (merge parallel FinFETs)
- Mode 3: high-V_{th} AND operation (merge series FinFETs)

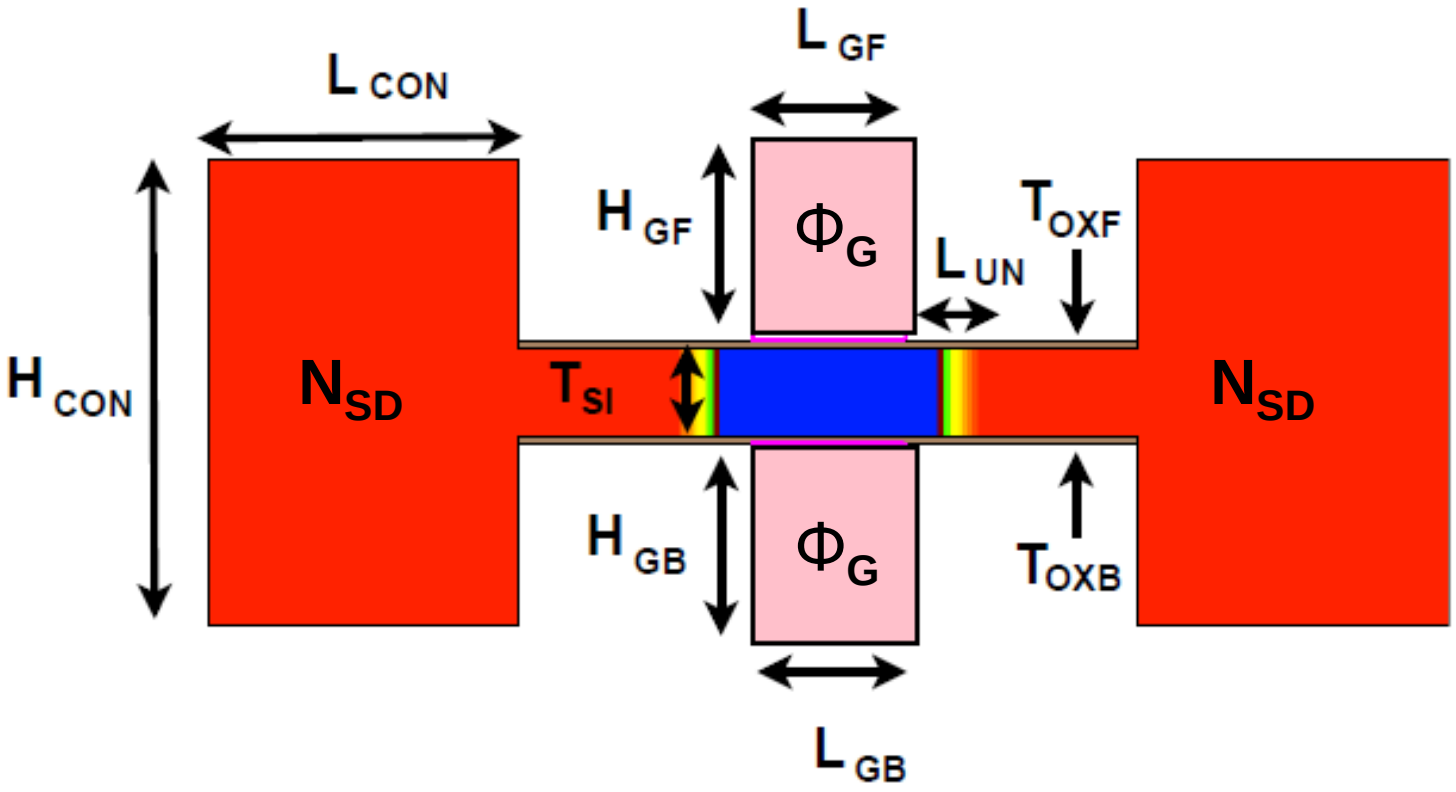


Low-V_{th} (IG) (SG) High-V_{th} (IG)

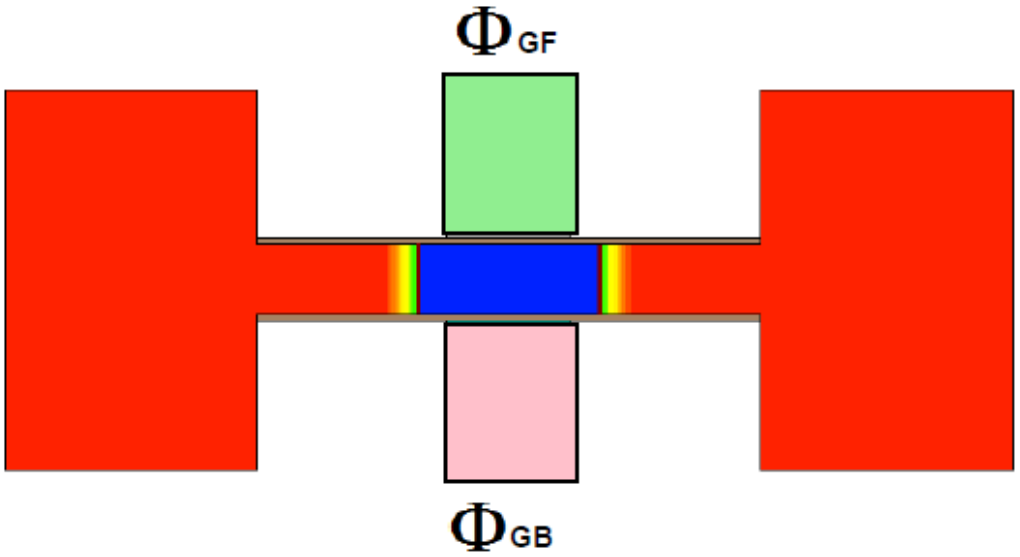
	t_{ox} (nm)		ϕ (eV)		t_{Si} (nm)		l_u(nm)		V_{th} (V)			
									SG		IG	
	L	H	L	H	L	H	L	H	L	H	L	H
n-type	1	2	4.5	4.8	12	6	3	5	0.18	0.3	0.54	0.97
p-type	1	2	4.85	4.5	12	6	3	5	0.09	0.16	0.5	0.95

(Rostami-Mohanram, 2010)

FinFET: 2D Cross-section



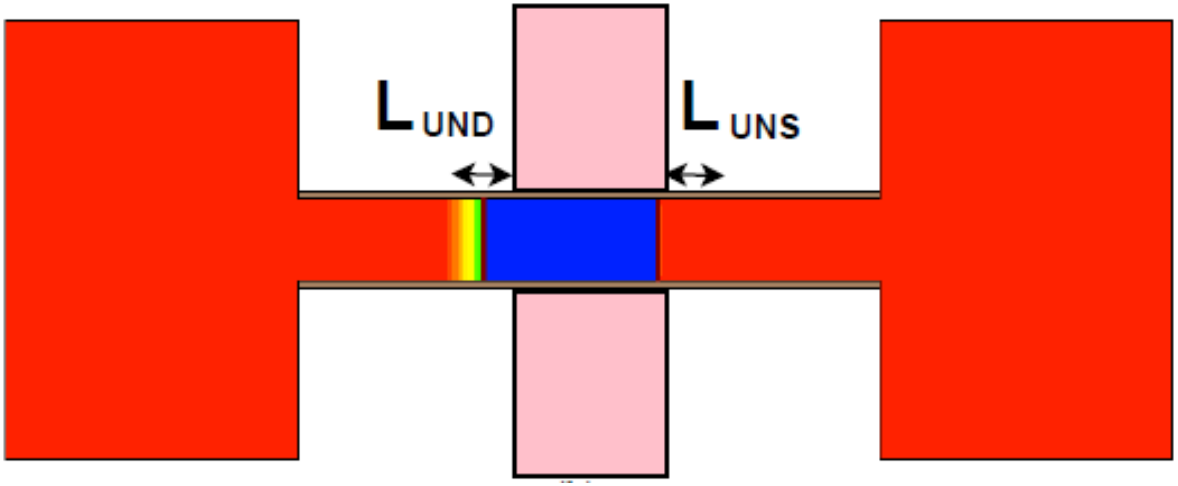
Asymmetric FinFETs: AWSG



Fabricated by IBM

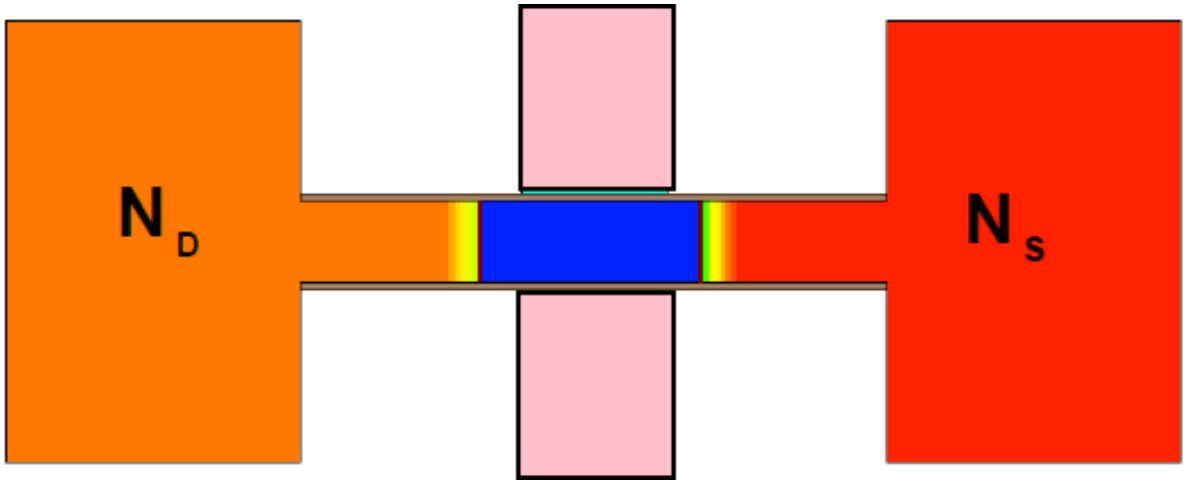
- Different gate workfunctions
- Very low leakage: 160X lower than symmetric SG
  - Price paid: 1.3X lower I_{on} than symmetric SG

Asymmetric FinFETs: AUSG



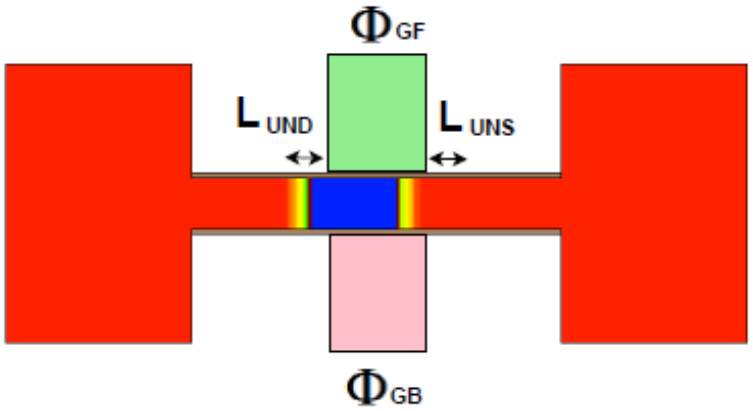
- Different gate underlaps
- Higher I_{on}: 1.3X higher than symmetric SG
  - Price paid: 2.2X higher leakage than SG

Asymmetric FinFETs: ADSG

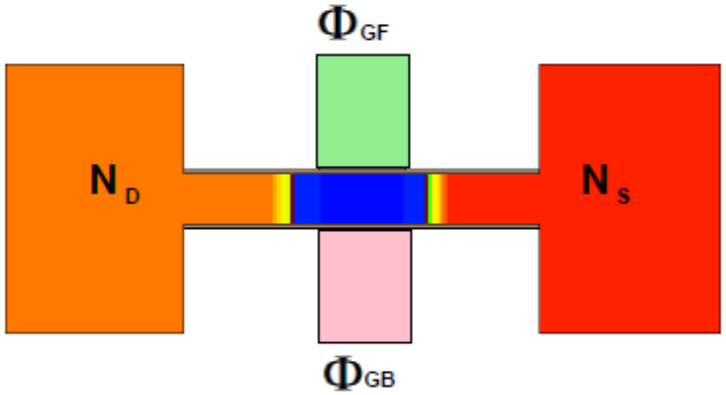


- Different drain-source doping
- Lower leakage: 1.4X lower than symmetric SG
  - Price paid: 1.6X lower I_{on} than symmetric SG

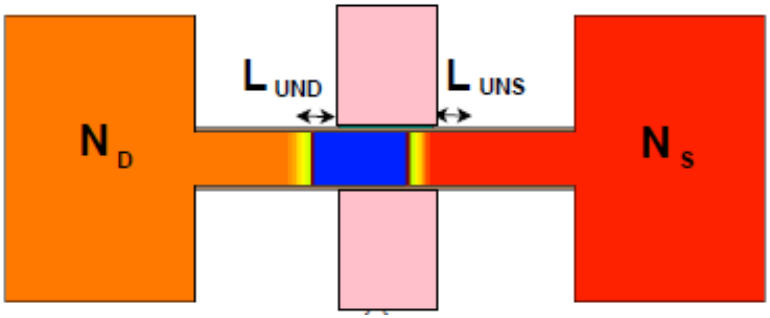
Multi-parameter Asymmetric FinFETs



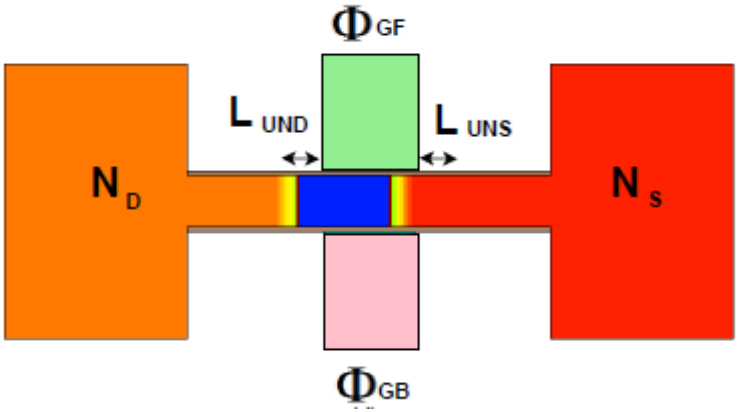
AWUSG



AWDSG



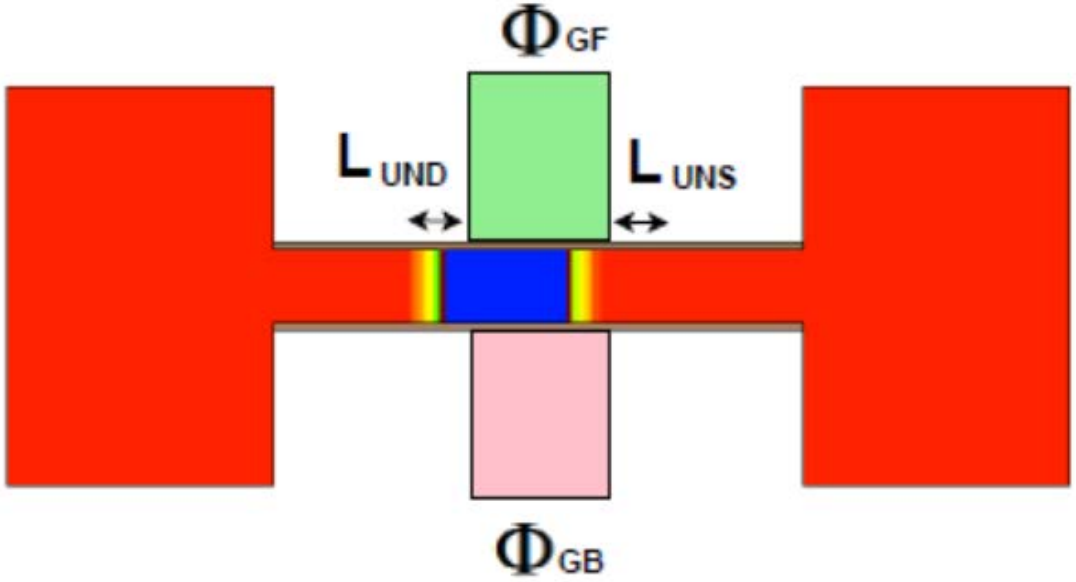
AUDSG



AWUDSG

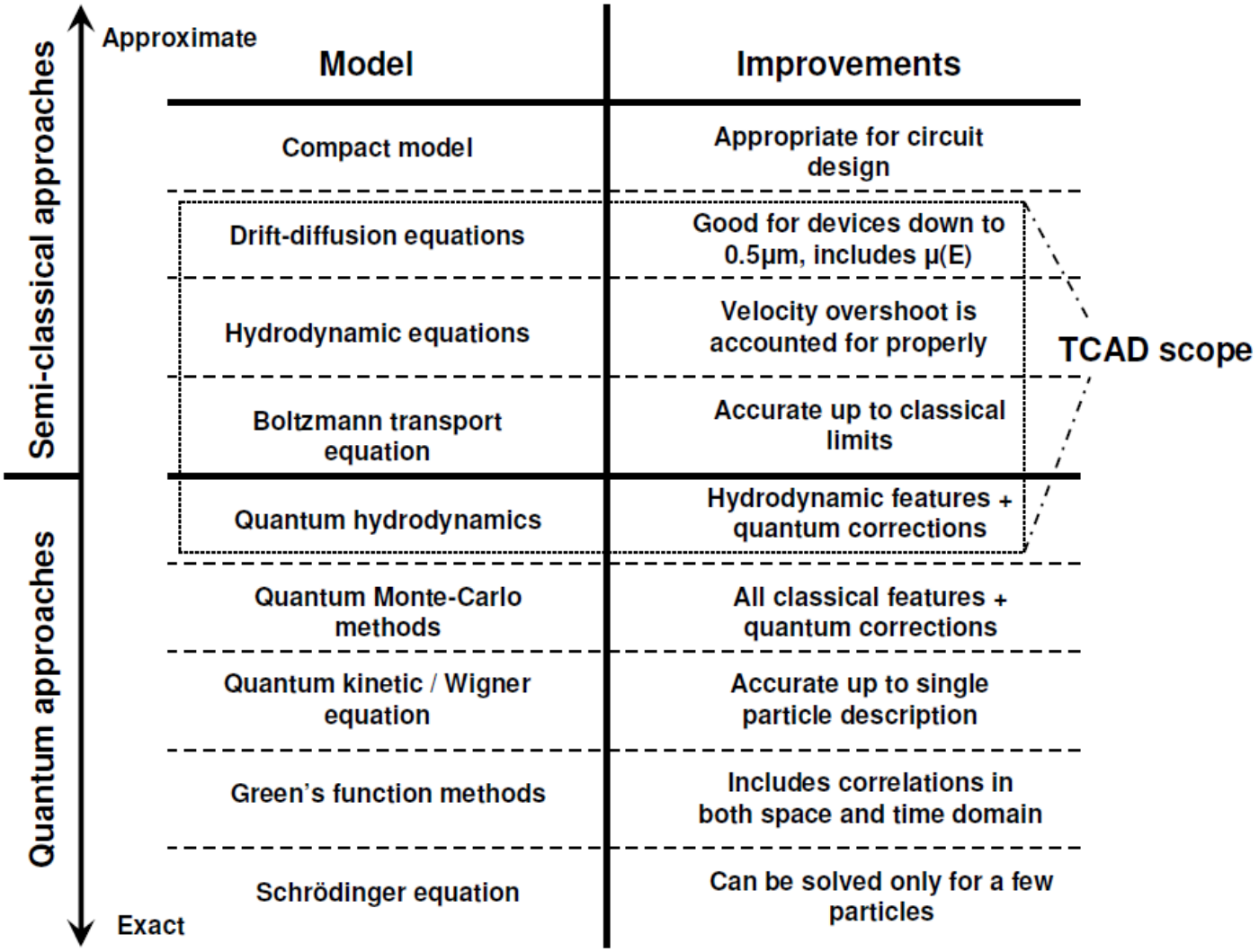
(Chaudhuri-Jha, 2016)

AWUSG: Best I_{on}/I_{off} Characteristics

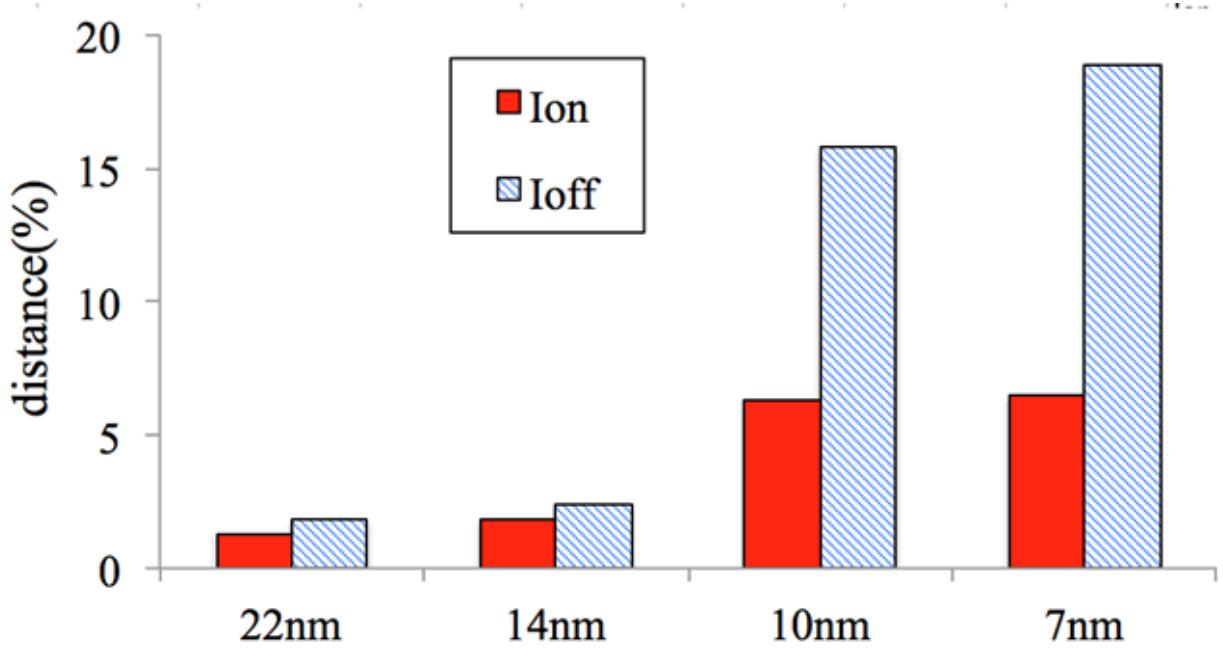


- Lower leakage: 16X lower than symmetric SG
- Better I_{on}: 10% higher than symmetric SG

Challenge 3: Device Simulation



Need for Quantum Hydrodynamic Model

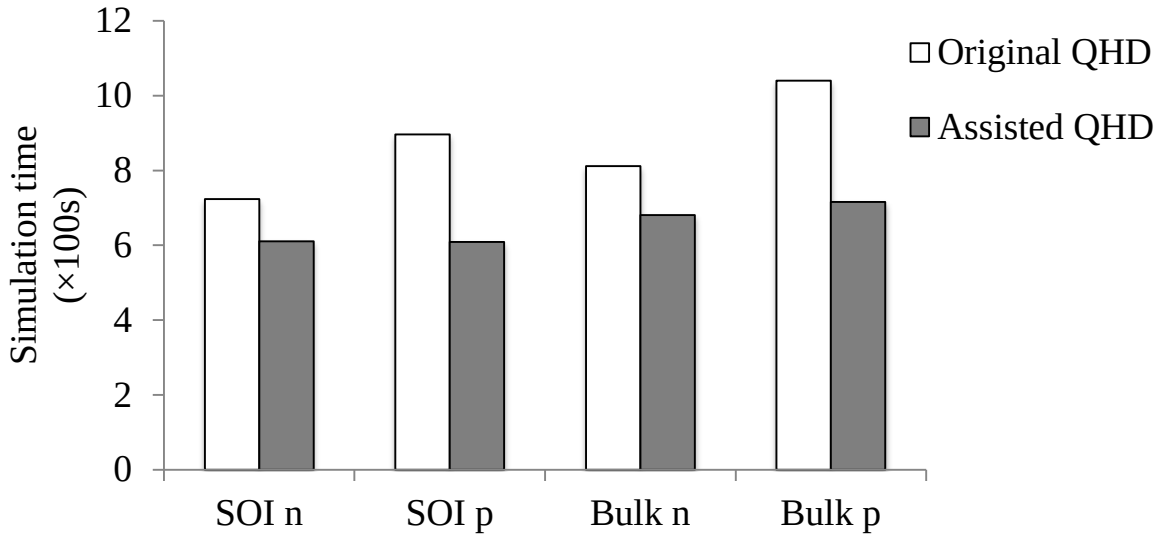


Error of hydrodynamic model vs. quantum hydrodynamic model

Quantum Hydrodynamic Model (Contd.)

- Challenge: Quantum hydrodynamic model has poor convergence rates
- Overcoming the challenge: reuse device states from a simpler transport model as initial guess for a more complex transport model
  - Drift-diffusion -> hydrodynamic -> quantum hydrodynamic
- Opportunity: makes it possible to explore optimal FinFET parameter values (gate length, fin thickness, oxide thickness, workfunction, etc.) at advanced (10nm, 7nm) technology nodes

Quantum Hydrodynamic Model (Contd.)



CPU time cost improvement

Simulation type →	Original QHD	Assisted QHD
FinFET type	Non-convergence rate	
SOI n	1.0%	0%
SOI p	0.2%	0.2%
Bulk n	16.3%	1.7%
Bulk p	1.8%	0.8%

Convergence behavior improvement

(Dai-Jha, 2016)

Device Simulation: Huge Runtimes

- Challenge: 3D device simulation of a FinFET may take from 0.5 hour to several CPU hours
  - Thousands of FinFET device simulations for each FinFET variant under process-voltage-temperature (PVT) variations may take several CPU months
- Overcoming the challenge:
  - Adjust underlap of 2D cross-section to mimic 3D device simulation (two orders of magnitude speedup)
  - Use device state of nominal device to simulate FinFETs under PVT variations (another order of magnitude speedup)

(Chaudhuri-Jha, 2016)

Quo Vadis FinFET Standard Cells and Logic Circuits?

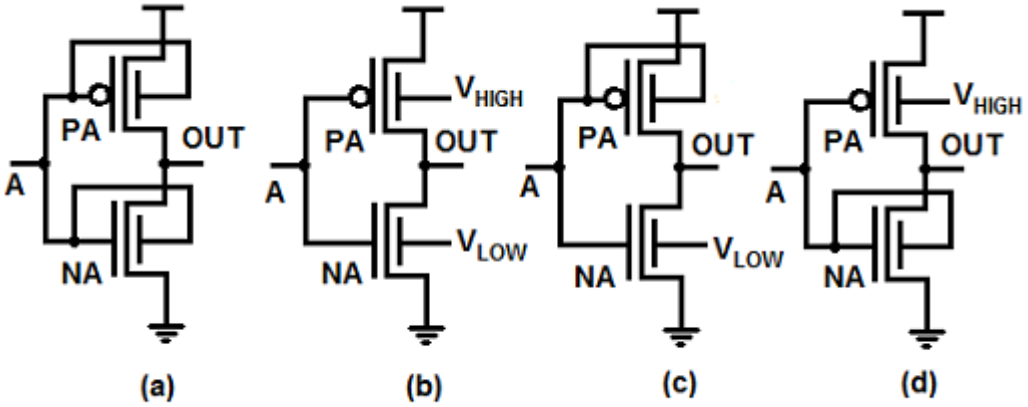
Standard Cell Possibilities

- Interesting FinFETs: SG, IG, AWSG, AWUSG
- Hybrid FinFET inverters: 16 combinations
- Hybrid 4T NAND gates: 256 combinations

- Opportunity: explore hybrid standard cells and obtain non-dominated cells in the area-delay-leakage space

Hybrid SG/IG Inverter Examples

- IGn → IG-mode nFinFET, IGp → IG-mode pFinFET
- Dominated inverter: IGp



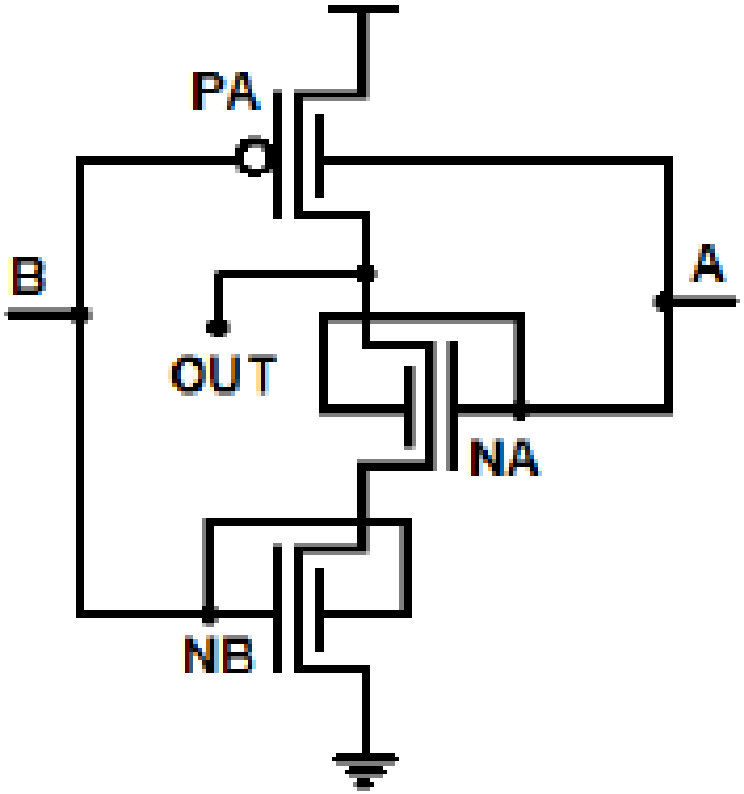
INV: (a) SG (b) LP (c) IGn (d) IGp

Topology	SG	LP	IGn	IGp
Area (w.r.t to SG)	1	1.36	1.36	1.36
Avg. I_{LEAK} (nA)	2.51	0.12	0.33	2.31
t_p (ps)	3.31	12.15	5.55	9.66

(Bhoj-Jha, 2011)

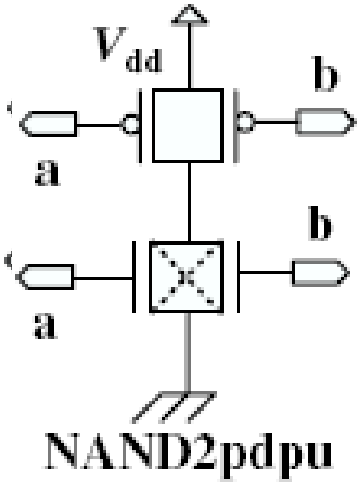
Hybrid 3T NAND Gate

- Use of low-V_{th} IG pFinFET for OR operation

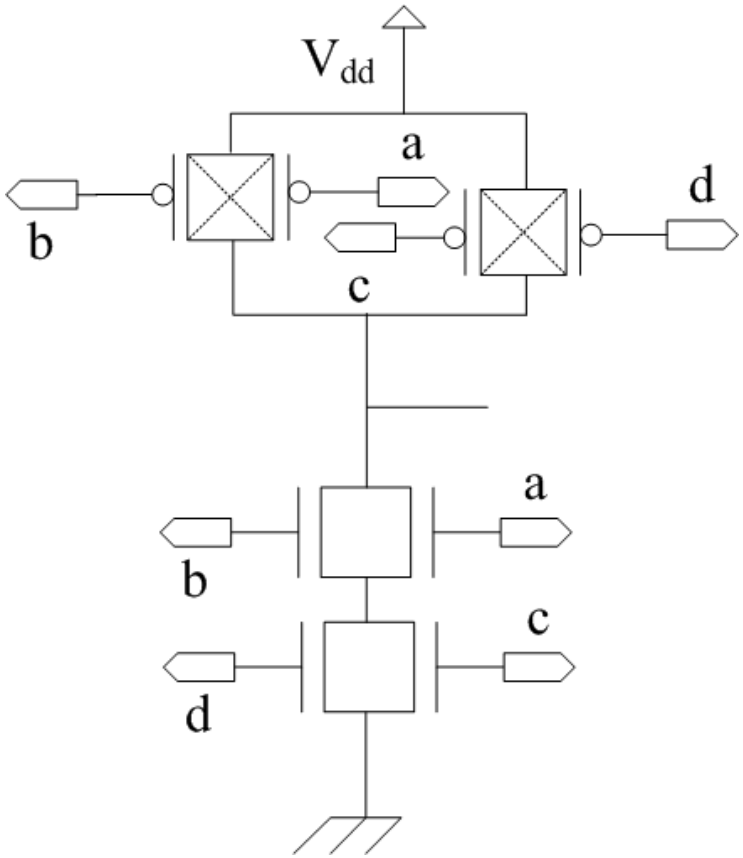


(Muttreja-Jha, 2007)

Opportunity: AND-FinFETs



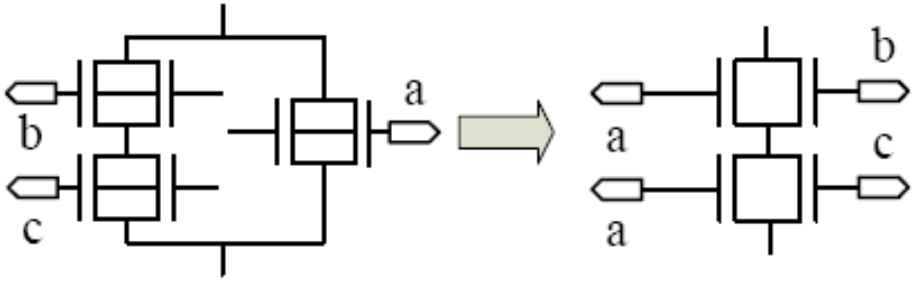
Two-transistor NAND



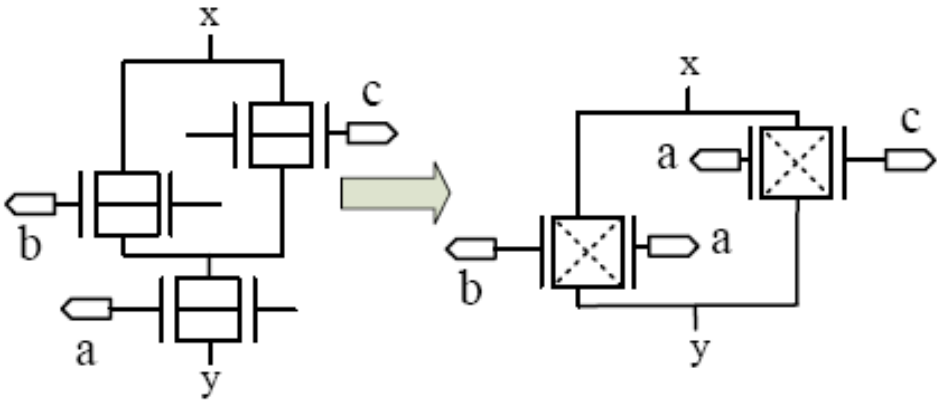
Four-transistor implementation of
[(a+b)(c+d)]'

(Rostami-Mohanram, 2010)

Defactoring



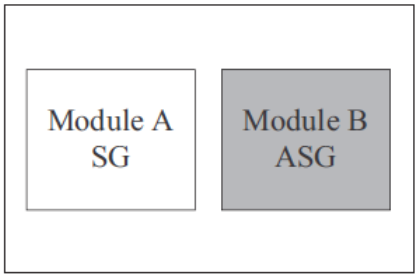
a + bc → (a+b)(a+c)



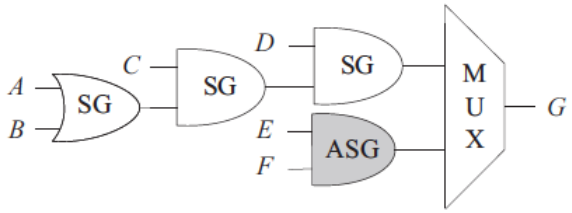
a(b+c) → ab + ac

Hybrid Approach at Different Levels

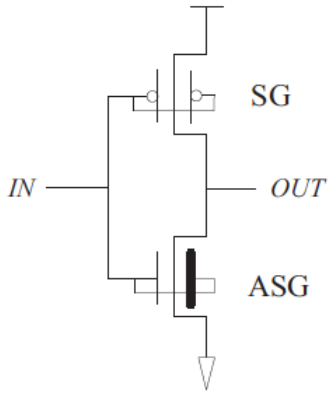
- Four levels
  - (a) Architecture
  - (b) Circuit
  - (c) Logic gate
  - (d) Transistor
- Choosing levels
  - From (a) to (d): More leakage power reduction, but more complex design



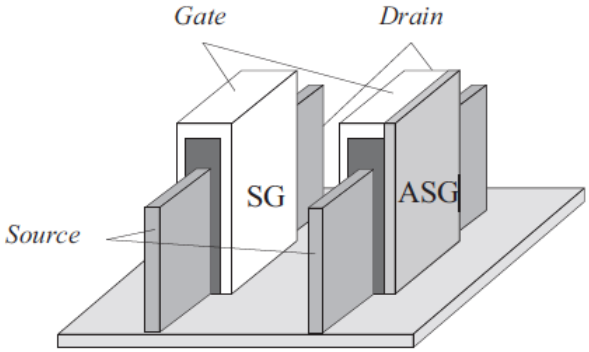
(a)



(b)



(c)



(d)

(Chen-Jha, 2014)

AWSG/AWUSG vs. SG Standard Cells

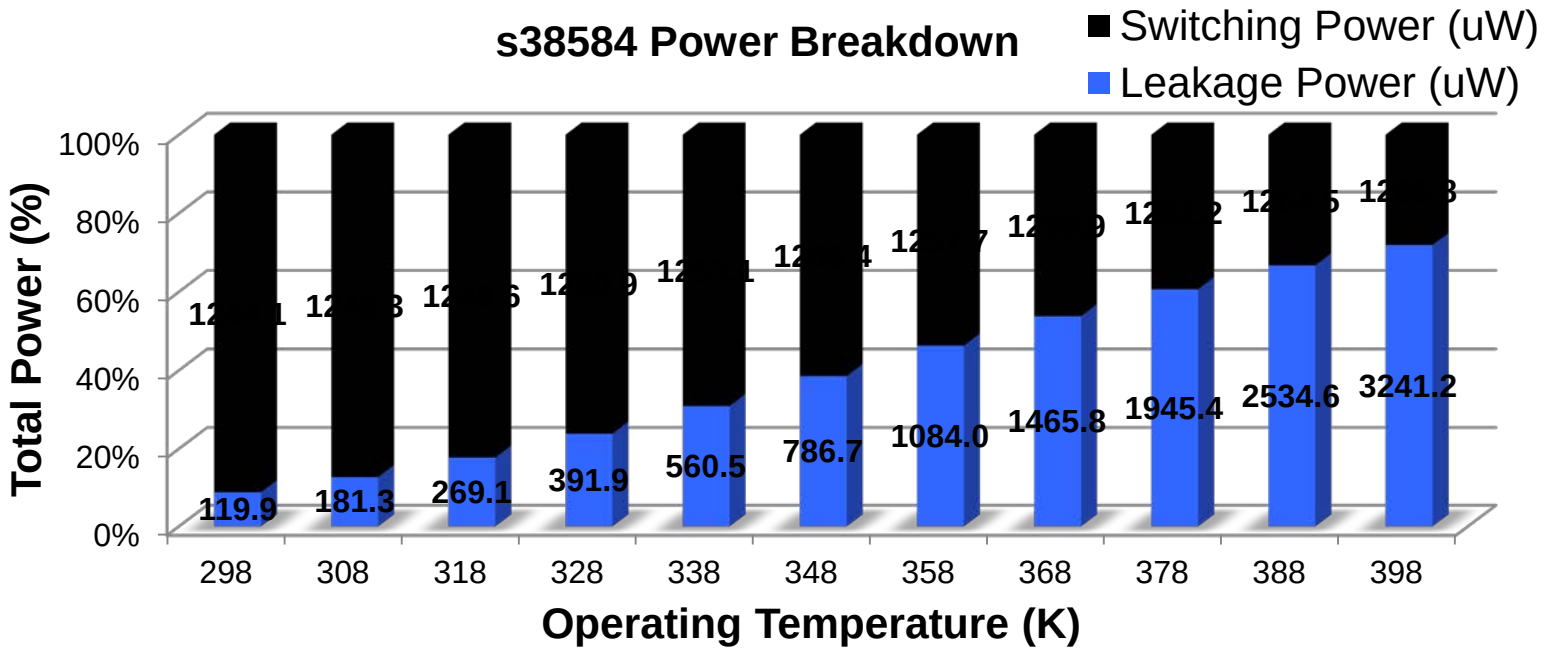
- AWSG vs. SG standard cells (T = 348K)
  - Area: 1X
  - Delay: 1.3X higher
  - Leakage: 33X lower
- AWUSG vs. SG standard cells
  - Area: 1X
  - Delay: 1.15X lower
  - Leakage: 12X lower

AWSG/AWUSG vs. SG Logic Circuits

- Hybrid AWSG/SG vs. SG logic circuits (ISCAS'89)
  - Delay: 1X
  - Area: 1.12X higher
  - Total power: 1.47X lower
- AWUSG vs. SG logic circuit
  - Delay: 1X
  - Area: 1.16X lower
  - Total power: 1.40X lower

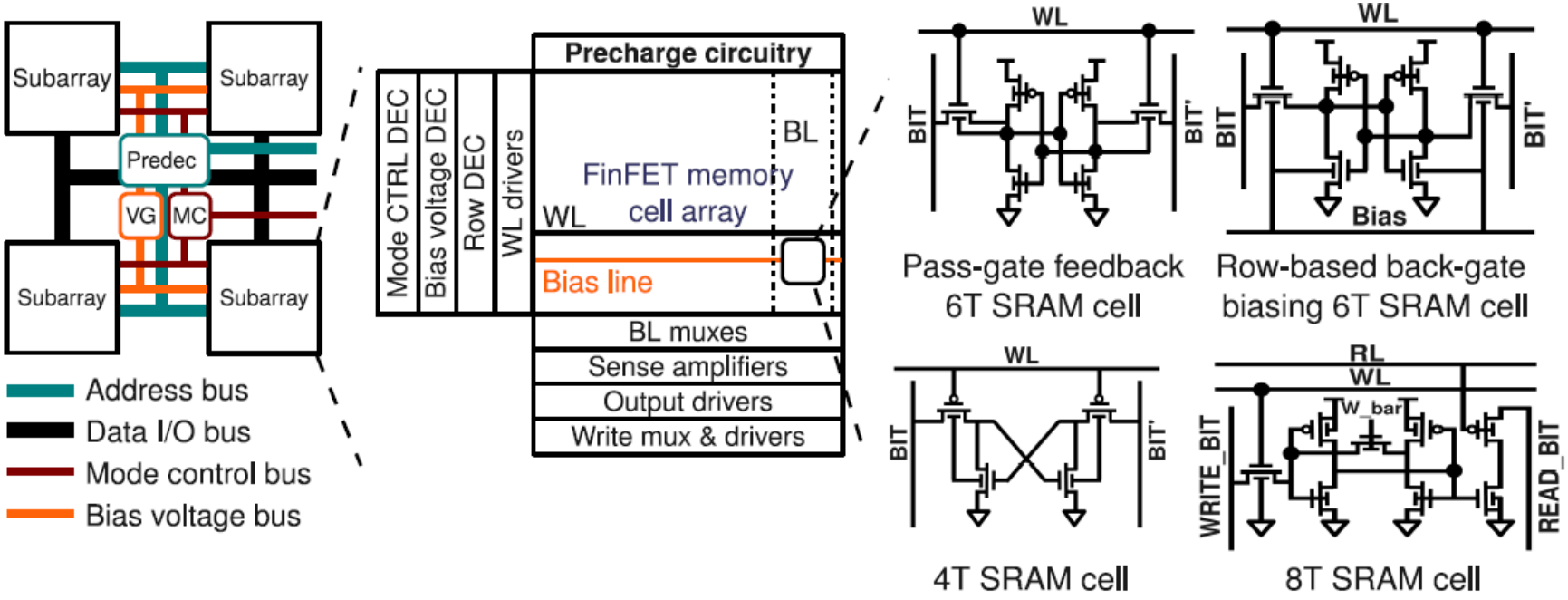
Impact of Temperature

- Impact of temperature increase from 298K to 398K
  - Delay increases by 5%
  - Leakage/total power ratio increases from 9% to 72%
  - Switching power only increases by 2%
- Implication
  - Obtain temperature at which leakage in equilibrium



Use of FinFET Variants to Address the Power Wall

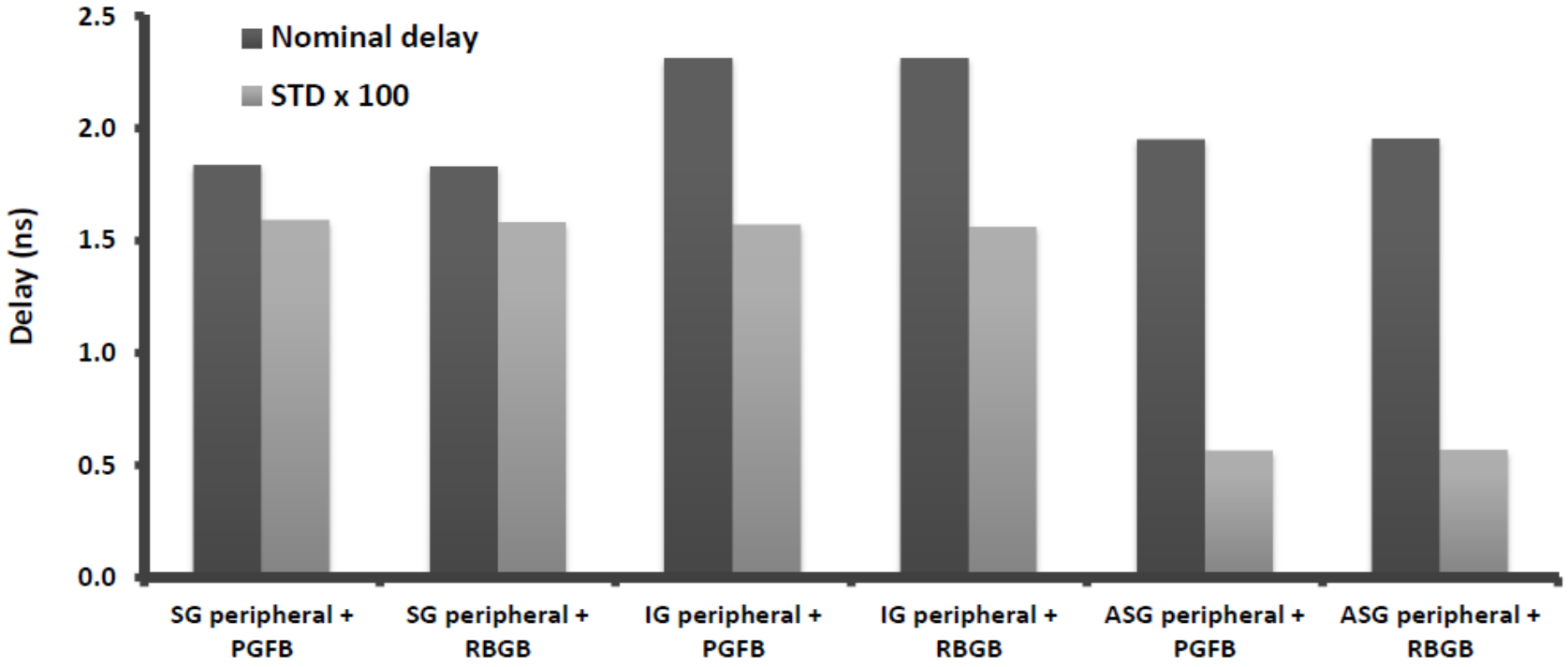
FinFET Cache



Cache Delay and Leakage

- Cache configuration
  - 4MB cache (Default: SG-mode peripheral components + PGFB cells)
  - Block size: 64 bytes
  - Associativity: 4
  - Number of banks: 4
- L2 cache leakage: known to be a large fraction of chip multiprocessor power consumption

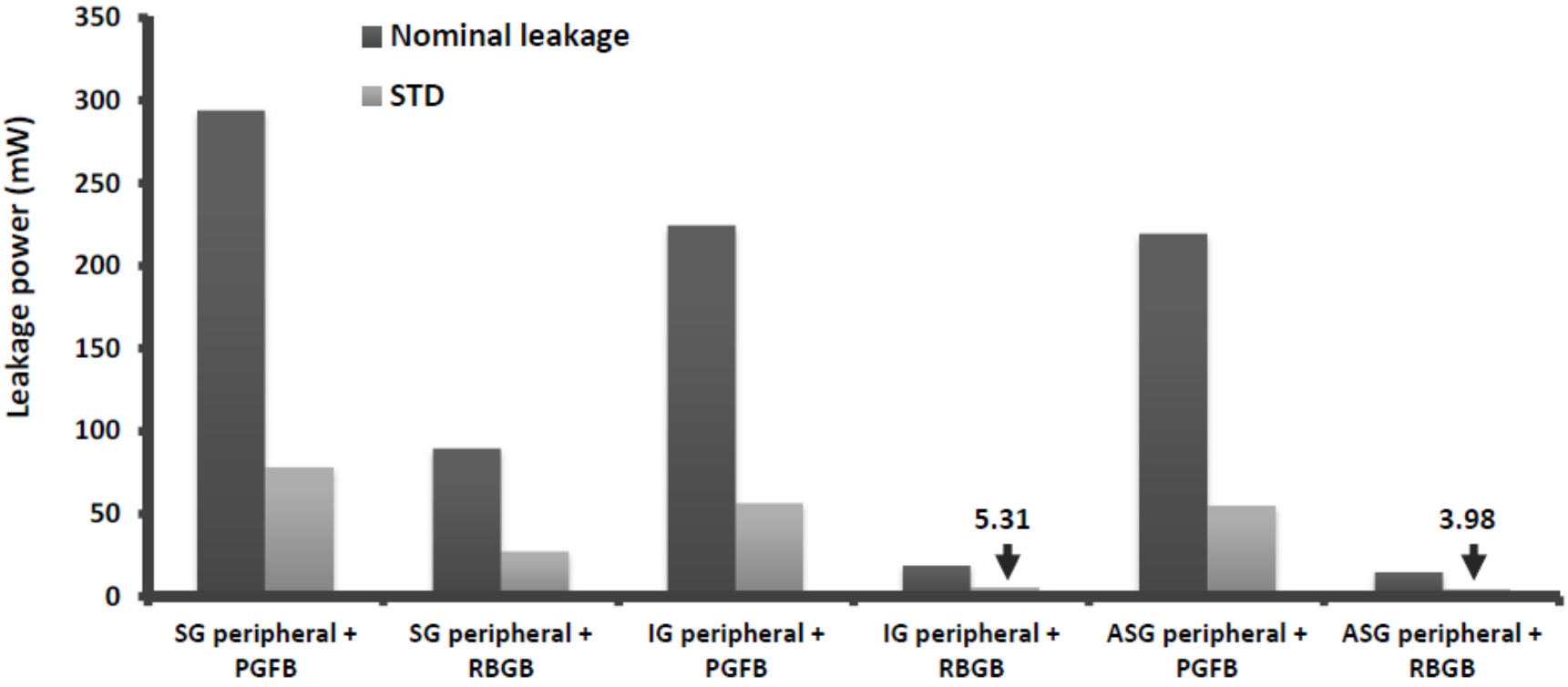
Comparison of FinFET Design Styles



Delay comparison

(Lee-Jha, 2014)

Comparison of Design Styles (Contd.)



Leakage comparison

Hybrid CMP Design

- CMP
  - Eight Cores
  - 4MB shared L2 cache
  - Hybrid SG/AWSG execution units
  - Hybrid SRAM
    - AWSG SRAM cell
    - AWSG/SG decoder
    - Remaining peripherals: SG
- Power impact relative to pure SG FinFET design
  - Leakage power: 10.0X lower
  - Total power: 4.1X lower
  - Performance: same

Conclusions

- FinFET device variants: offer much wider choices for area-delay-leakage tradeoffs than CMOS
  - Enable a lateral move from traditional FinFET to variant at the same technology node
  - Novel circuits and architectures possible
- FinFET device simulation: traditional transport models no longer accurate
- Power wall: can be pushed back with FinFET variants

FinFET Tools Available from Princeton

- FinPrin: statistical timing/power analysis
- GenFin: statistical logic circuit optimization
- Architectural power/performance/yield analysis
  - gem5-PVT: chip multiprocessor
  - McPAT-PVT: processor core
  - FinCANON: cache and network-on-chip