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## Energy Efficient & Secure Computing in Nanoscale CMOS

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Future computing systems spanning exascale supercomputers to wearable devices demand orders of magnitude improvements in energy efficiency while providing desired performance. The system-on-chip (SoC) designs need to span a wide range of performance and power across diverse platforms and workloads. The designs must achieve robust near-threshold-voltage (NTV) operation in nanoscale CMOS process while supporting a wide voltage-frequency operating range with minimal impact on die cost. We will discuss circuit and design technologies to overcome the challenges posed by device parameter variations, supply noises, temperature excursions, aging-induced degradations, workload and activity changes, and reliability considerations. The major pillars of energy-efficient SoC designs are: (1) circuit/design optimizations for fine-grain multi-voltage & wide dynamic range, (2) fine-grain on-die power delivery & management, (3) dynamic adaptation & reconfiguration, (4) dynamic on-die error detection & correction, and (5) efficient interconnects. In addition, hardware security is becoming increasingly critical across all SoC platforms, especially with rapid growth of the Internet-of-Things (IoT). We will discuss key security circuit building blocks and efficient cryptographic accelerators in scaled CMOS process.

### **Biography:**

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 236 publications in refereed international conferences and journals and 202 patents, with 29 more patents filed (pending). He received an Intel Achievement Award for his contributions to an integrated voltage regulator technology. He received a Best Paper Award at the 1996 IEEE International ASIC Conference, and nominations for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC) and 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference (DAC) as one of the "Top 10 Cited Papers in 50 Years of DAC". He received a PhD in Electrical Engineering from Rensselaer Polytechnic Institute, Troy, New York. He is a Fellow of the IEEE.