Test Strategies for Sub-20nm Designs

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The rapid scaling of semiconductor devices along with technological innovations including material and process changes are changing the way ICs have to be tested in the future. Traditional fault models are being replaced by defect-aware transistor-level models; advanced compression techniques and hierarchical DFT are gaining momentum to address rising test costs and test implementation time; and there is significant ongoing investment towards using manufacturing test data for quickly isolating systematic defects thereby aiding fast yield ramp up. In this talk, I will focus on summarizing the test challenges for sub-20 nm designs and highlight some of the techniques being adopted by the industry to address these challenges.

Biography: Nilanjan Mukherjee received a B.Tech.(Hons) degree in Electronics & Communication Engineering from IIT, Kharagpur, and a Ph.D. degree from McGill University, Montreal, Canada. Dr. Mukherjee is currently the Engineering Director for the Test Synthesis Group in the Silicon Test Solutions division at Mentor Graphics. At Mentor Graphics, he was a co-inventor of the EDT technology and a lead developer for TestKompress®, which is the leading test compression tool in the industry today. Prior to joining Mentor Graphics, he worked at Lucent Bell Laboratories in New Jersey.

Dr. Mukherjee has co-authored 70+ technical papers at various conference proceedings and archival journals. He is a co-inventor of 39 US patents and several international patents. He has received numerous Best Paper awards including the Most Significant Paper Award at ITC 2012, the Best Paper Award at VLSID in 2009, the Donald O. Pederson Outstanding Paper Award from the IEEE Circuits and Systems Society in 2006, the Teruhiko Yamada Memorial Best Student Paper Award at ATS 2001, and the Best Paper Award at VTS 1995. Dr. Mukherjee has served on the program committee for various technical conferences and workshops. He has represented Mentor Graphics at the Semiconductor Research Organization (SRC), at the International Technology Roadmap for Semiconductors (ITRS), and as a panelist for National Science Foundation (NSF). Dr. Mukherjee has given several tutorials on DFT at DAC, ITC, and VLSI Design conferences, offered short term courses on DFT, and has given talks at various conferences and company sponsored events.