The 27th International Conference on VLSI Design

2014

The 13th International Conference on Embedded Systems

January 5-9, 2014, IIT Bombay, Mumbai , India

Call for Papers

http://vlsidesignconference.org

This joint conference is a forum for researchers and designers to present and discuss current topics in VLSI design, electronic design automation, embedded systems, and emerging technologies. Two days of tutorials will be followed by three days of regular paper sessions, special sessions, and embedded tutorials. Industry presentation sessions along with exhibits, panel discussions, Design Contest, and Education Forum round off the program.

TOPICS OF INTEREST: Papers are invited on previously unpublished results in the following categories:

1. **Embedded Systems**

Embedded system hardware/software co-design; Reconfigurable hardware design; Embedded software; Real-time operating systems; Middleware and virtualization; Embedded multi-cores and many-cores; Communications; Encryption, security, compression; Hybrid systems-on-chip; Sensor networks; Programmable devices; Hardware-software co-verification; Embedded system reliability; Embedded applications (automotive, mobile, medical, etc.), platforms, and case studies

2. Digital Design

Low-power design; Asynchronous design; Package and board design

3. Analog/RF Design

Low-power design; Analog, mixed-signal, and RF systems; Package and board design

4. System-level Design/ESL

System-level design methodology; Gigascale design methodology; Multicore systems; Processor and memory design; Concurrent interconnect; Networks-on-chip; Defect tolerant architectures

5. Logic Synthesis and Physical Design

Logic synthesis; Technology mapping; Asynchronous synthesis; Physical design; Floor planning; Placement; Routing; Clock Design; Layout issues in design for manufacturability

6. Test and Reliability

Fault modeling/simulation; ATPG; DFT; Delay test; Fault-tolerance; Online test; AMS/RF test; Board-level and system-level test; Silicon debug, post-silicon validation; Memory test; Reliability test

7. Functional Verification

Behavioral Simulation; RTL Simulation; Coverage Driven Verification; Assertion Based Verification; Gate-level simulation; Emulation; Hardware Assisted Verification; Formal Verification; Equivalence Checking; Verification Methodologies

8.evice/circuit simulation and modeling

Design verification; Signal integrity; Technology modeling-design-simulation; Analog/mixed-signal simulation; Multi-domain simulation; Numerical methods; Device modeling; Timing analysis; Asynchronous timing; Device/circuit level variability models; Reliability simulation

9.Emerging Technologies

Issues in nano-CMOS technologies; MEMS; CMOS sensors; CAD/EDA methodologies for nanotechnology; Non-classical CMOS; Post-CMOS devices; Biomedical circuits and systems

EMBEDDED TUTORIALS AND SPECIAL SESSIONS: Proposals in relevant emerging areas should be submitted as two-page abstracts. On acceptance, authors are required to submit full regular papers.

HALF-DAY AND FULL-DAY TUTORIALS: Continuing a tradition of running a highly successful series of tutorials, the first two days of the conference will be dedicated to tutorials on recent topics in VLSI design, EDA, VLSI technology, and embedded systems. Tutorial proposals on topics of attendee interest are invited.

PANELS: Proposals must be submitted with an abstract, and a list of panellists

SUBMISSIONS: All submissions should be made electronically via the conference website by July 24, 2013. Your manuscript should clearly state the novel ideas, results, and applications of the contribution. Paper submissions will undergo a double-blind review. Papers must be in PDF format and not exceed 6 single-spaced pages including figures and references in two-column IEEE conference paper format. Papers exceeding the page limit or identifying the authors will be rejected without review. **EXHIBITS**: Please contact the Exhibits Chair to explore opportunities for companies to display their products/services.

FELLOWSHIPS: The conference will award fellowships, based on need and merit, to partially cover expenses of attendees from India. Application details will be posted at the conference website.

DESIGN CONTEST: Please check the conference website or contact the Design Contest Chair for more details.

IMPORTANT DATES:

Submission of Abstract deadline: **Submissions Closed**

Submission of Full paper deadline: **Submissions Closed**

Acceptance of notification : **October 2, 2013**

Camera ready paper due : **October 10, 2013**