27th International Conference on VLSI Design 2014

13th International Conference on Embedded Systems

5th International Workshop on Reliability Aware System Design and Test

Tutorial Schedule

January 5 (Sunday) Tutorials					
9:00 am – 12:00 noon	Tutorial T1: Ambient Intelligence through Internet of things - An application development approach	Tutorial T2A: Scheduling Issues in Embedded Real-Time Systems	Tutorial T3A: Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices		
1:00 pm – 4:00 pm		Tutorial 2B: Cost/Application/Time to Market Driven SoC Design and Manufacturing Strategy	Tutorial T3B: Engineering Change Order (ECO) phase Challenges and Methodologies for High Performance Design		
January 6 (Monday) Tutorial					
9:00 am – 12:00 noon	Tutorial T4: All you Need to know about hardware Trojans and Counterfeit ICs Presenters:	Tutorial T5: Microfludic BioChips: Connecting VLSI and Embedded Systems to the Life Science	Tutorial T6A: Pedagogy of Negative Feedback Circuits	Tutorial T7A: Techniques for Network-on-Chip Design and Test	Tutorial T8A: Realization of RF Front-End for a Cognitive Radio
1:00 pm – 4:00 pm			Tutorial T6B: Embedded Memory Design for Future Technologies: Challenges and Solutions	Tutorial T7B: Network on Chips - The Journey Overview	

Main Conference

January 7 (Tuesday)						
9:00 am – 10:45 am	INAUGURATION PLANARY – 1					
10:45am – 11:15 am	Coffee Break					
11:15 am – 12:45 pm	PLANARY– 2					
12:45 pm – 2:00 pm	Lunch Break					
2:00 pm – 2:30 pm	Keynote Talk – 1					
2:40 pm – 4:00 pm	A-1 3DT	B-1 RT	C-1 FP	D-1 RC	E-1	F-1
4:00 pm – 4:30 pm	COFFEE					
4:30 pm – 6:30 pm	A-2 SA	B-2 EP	C-2 LP	D-2 LC	E-2	F-2
6:30pm – 7:30 pm	Ph.D Forum & Poster Session					
7:30 pm – 8:30 pm	Banquet Talks					
8:30 pm – 10:30 pm	Banquet					
January 8 (Wednesday)						
9:00 am – 10:30 am	PLANARY – 3					
10:30 am – 11:10 am	COFFEE					
11:10 am – 1:10 pm	A-3 DV	B-3 AR	C-3 DD	D-3 MB	E-3	F-3
1:10 pm – 2:30 pm	LUNCH					
2:30 pm – 3:00 pm	Keynote Talk – 2					
3:10 pm - 4:30 pm	A-4 TG	B-4 NC	C-4 PD	D-4 AC-1	E-4	F-4

4:30 pm – 5:30 pm	COFFEE (Poster Session)					
5:30 pm – 6:30 pm	Panel Discussion					
7:00 pm – 9:00 pm	Cultural Program & Award Ceremony					
9:00 pm – 10:30 pm	Banquet					
January 9 (Thursday)						
9:00 am – 10:30 am	PLANARY – 4					
10:30 am – 11:10 am	Coffee Break					
11:10 am – 1:10 pm	A-5 RL	B-5 MP	C-5 MS	D-5 ET	E-5	F-5
1:10 pm – 2:30 pm	LUNCH					
2:30 pm – 3:30 pm	Inauguration of RASDAT 2014 JOINT RASDAT & VLSI DESIGN PLANARY SESSION					
3:30 pm – 4:00 pm	Coffee Break					
4:00 pm - 6:00 pm	A-6 Mm	B-6 ES	C-6 MA	D-6 AC-2	E-6	RASADT Session S1
6:00 pm – 7:00 pm	RASDAT Panel Discussion					
7:00 pm – 8:00 pm	Cultural Program for RASDAT					
8:00 pm – 10:00 pm	Banquet for RASDAT					
January 10 (Friday) RASDAT						
9:00 am – 10:30 pm	PLANARY SESSION - 2					
10:30 am – 11:00 am	Coffee Break					
11:00 am – 12:30 pm	Technical Session S2					

12:30 pm – 1:30 pm	Lunch Break
1:30 pm – 3:00 pm	PLANARY SESSION - 3
3:00 pm – 3:30 pm	Coffee Break
3:30 pm – 5:00 pm	Technical Session - S3
5:00 pm – 5:15 pm	Closing

Sessions:
3DT: 3D Test
SA: SAT Application
TG: Test Generation
RL: Reliable Circuits
DV: Design Verification
LP: Low Power Design
FP: FPGA
EP: Embedded Platform
RT: Real Time Systems
AR: Architectures
NC: Network on Chip (NoC)
MP: MPSoC
ES: Embedded Systems
DD: Digital Design
MS: Modeling and Simulations
MA: Modeling and Analysis
LC: Low Power Circuits
RC: RF Circuits
AC: Analog Circuits
MB: MEMS & Biochips
ET: Emerging Technology

Track A: TESTING & RELIABILITY

3D TEST (A-1)

[319] Spencer Millican and Kewal Saluja. A Test Partitioning Technique for Scheduling Tests for Thermally Constrained 3D Integrated Circuits

[383] Eshan Singh. Analytical Modeling of 3D Stacked IC Yield from Wafer to Wafer Stacking with Radial Defect Clustering

[30] Nima Aghaee, Zebo Peng and Petru Eles. Process-Variation Aware Multi-Temperature Test Scheduling

[134] Subhendu Roy and David. Z. Pan. Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown

SAT APPLICATION (A-2)

[42] Mehdi Dehbashi and Görschwin Fey. Debug Automation for Synchronization Bugs at RTL

[278] Kun Bian, D. M. H. Walker and Sunil Khatri. Techniques to Improve the Efficiency of SAT based Path Delay Test Generation

[369] Alexander Czutro, Ilia Polian, Sudhakar M. Reddy and Bernd Becker. SAT-Based Test Pattern Generation with Improved Dynamic Compaction

[368] Matthias Sauer, Sven Reimer, Sudhakar M. Reddy and Bernd Becker. Efficient SAT-based Circuit Initialization for Large Designs

DESIGN VERIFICATION (A-3)

[140] David Sheridan, Lingyi Liu, Hyungsul Kim and Shobha Vasudevan. A Coverage Guided Mining Approach for Automatic Generation of Succinct Assertions

[156] Pradeep Kumar Nalla, Rajkumar Gajavelly, Jason Baumgartner, Hari Mony and Robert Kanzelman. Effective Liveness Verification using a Transformation-Based Framework

[159] Mohammadhashem Haghbayan, Bijan Alizadeh, Majid Namaki and Saeed Safari. Formal Verification and Debugging of Array Dividers With Auto-Correction Mechanism

[324] Yinlei Yu, Pramod Subramanyan, Nestan Tsiskaridze and Sharad Malik. All-SAT using Minimal Blocking Clauses

TEST GENERATION (A-4)

[318] Spencer Millican, Kewal Saluja and Parameswaran Ramanathan. Providing Encrypted Intellectual Property Cores with Logic and Fault Simulation Capabilities

[135] Sharada Jha, Kameshwar Chandrasekar, Weixin Wu, Ramesh Sharma, Sanjay Sengupta and Sudhakar Reddy. A Cube-aware compaction method for Scan ATPG

[387] Xiaoke Qin and Prabhat Mishra. Scalable Test Generation by Interleaving Concrete and Symbolic Execution

[567] Rahul Shukla, Phong Loi, Kathy Yang, Ken Pham, Arie Margulis and Nagesh Tamarapalli. Application of Test-View Modelling to Hierarchical ATPG

RELIABLE CIRCUITS (A-5)

[27] Nandakishor Yadav, Sunil Dutt and G. K. Sharam. A New Sensitivity-Driven Process Variation Aware Self-Repairing Low-Power SRAM

[257] Jayaram Natarajan, Sahil Kapoor, Debesh Bhatta, Adit Singh and Abhijt Chatterjee. Aggressive Timing Variation Adaptive Pipeline Design: Using Probabilistic Activity Completion Sensing With Backup Error Resilience

[353] B Naveen Kumar Reddy, Chandra Sekhar Mummidi, Sreehari Veeramachaneni and M B Srinivas. A Novel Low Power Error Detection Logic for Inexact Leading Zero Anticipator in Floating Point Units

[418] Ravi Kanth Uppu, Ravi Tej Uppu, Adit Singh and Illia Polian. Better-than-Worst-Case Timing Design with Latch Buffers on Short Paths

MEMORY (A-6)

[123] Sudhanshu Khanna, Satyanand Vijay Nalam and Benton Calhoun. Pipelined Non-Strobed Sensing Scheme for Lowering BL Swing in Nano-scale Memories

[198] Viveka K R and Bharadwaj Amrutur. Energy Efficient Memory Decoder Design for Ultra-Low Voltage Systems

[327] Prashant Dubey, Gaurav Ahuja, Sanjay Kumar Yadav, Vaibhav Verma and Amit Khanuja. A 500 mV to 1.0 V 128 Kb SRAM in Sub 20~nm Bulk-FinFET using auto-adjustable write assist

[573] Ignatius Bezzam and Shoba Krishnan. Minimizing Power and Skew in VLSI-SoC Clocking With Pulsed Resonance Driven De-skewing Latches

Track B: EMBEDDED SYSTEMS & SYSTEM LEVEL DESIGN

REAL TIME SYSTEMS (B-1)

[279] Mingsong Chen, Fan Gu, Lei Zhou, Geguang Pu and Xiao Liu. Efficient Two-Phase Approaches for Branch-and-Bound Style Resource Constrained Scheduling

[565] Hsiang-Kuo Tang, Parmesh Ramanathan and Katherine Morrow. Inserting Placeholder Slack to Improve Run-Time Scheduling of Real-Time Tasks in Heterogeneous Systems

[272] Santu Sardar and K. Anand Babu. Hardware Implementation of Real-Time, High Performance, RCE-NN based Face Recognition System

EMBEDDED PLATFORM (B-2)

[249] Marcelo Trindade Rebonatto, Fabiano Passuelo Hessel and Luiz Eduardo Schardong Spalding. EME Electric Supervision embedded on gas panel with microshock dangerousness degree

[364] Singamala Sudhakar, Manfred Brandl, Sandeep Vernekar, Veeresh Babu Vulligaddala, Ravikumar Adusumalli and Vijay Yadgiri Ele. Design of AFE and PWM drive for Lithium-ion battery management system for HEV/EV system

[142] E.M.T. Sirisha, T Sridevi and D Thirugnana Murthy. Process Disturbance Analyzer for Nuclear Reactor

[84] Manoj Kumar Misra, N. Sridhar and D. Thirugnana Murthy. Design and Implementation of Safety Logic with Fine Impulse Test System for Reactor Shutdown System of Indian Prototype Fast Breeder Reactor

ARCHITECTURES (B-3)

[2] Rance Rodrigues, Israel Koren and Sandip Kundu. Performance and Power Benefits of Sharing Execution Units between a High Performance Core and a Low Power Core. Univ. of Massechuseets

[31] Arun Joseph and Nagu Dhanwada. Process Synchronization in Multi-core Systems Using On-Chip Memories

[394] Xiaoke Qin and Prabhat Mishra. TECS: Temperature- and Energy-Constrained Scheduling for Multicore Systems

[479] Jyoti Gajrani, Pooja Mazumdar, Bernard Menezes and Sampreet Sharma. Challenges in implementing cache-based side channel attacks on modern processors

NETWORK-ON-CHIP (B-4)

[18] César Marcon, Ramon Fernandes, Rodrigo Cataldo, Fernando Grando, Thais Webber and Ana Benso. Tiny NoC: A 3D Mesh Topology with Router Channel Optimization for Area and Latency Minimization

[143] Tejasi Pimpalkhute and Sudeep Pasricha. NoC Scheduling for Improved Application-Aware and Memory-Aware Transfers in Multi-Core Systems

[221] Manoj Kumar, Vijay Laxmi, Manoj Gaur, Seok-Bum Ko and Mark Zwolinski. CARM: Congestion Adaptive Routing Method for On Chip Networks

[231] Bhanu Singh, Arunprasath Shankar, Francis Wolff, Daniel Weyer, Bhanu Negi and Christos Papachristou. Knowledge-Guided Methodology for Third-Party Soft IP Analysis

MPSOC (B-5)

[254] César Marcon and Thais Webber. Pre-Mapping Algorithm for Heterogeneous MPSoCs

[456] Farhad Merchant, Anupam Chattopadhyay, Ganesh Garga, S K Nandy and Ranjani Narayan. Efficient QR Decomposition Using Low Complexity Column-wise Givens Rotation (CGR)

[68] Rehan Ahmed, Parameswaran Ramanathan and Kewal Saluja. Temperature Minimization Using Power Redistribution in Embedded Systems

[287] Nishit Kapadia and Sudeep Pasricha. Process Variation Aware Synthesis of Application-Specific MPSoCs to Maximize Yield

EMBEDDED SYSTEMS (B-6)

[10] Wim Meeus, Tom Vander Aa, Praveen Raghavan and Dirk Stroobandt. Hard versus Soft Software Defined Radio

[235] Vikas Vij, Raghu Prasad Gudla and Kenneth Stevens. Interfacing Synchronous and Asynchronous domains for Open Core Protocol

[530] Brajendra Kumar Singh, Kemal Tepe and Mohammed Khalid. Control mechanism to solve false blocking problem at MAC layer in Wireless Sensor Networks

[554] Amit Pande, Shaxun Chen, Prasant Mohapatra and Gaurav Pande. Architecture for Blocking Detection in Wireless Video Source Authentication

Track C: DIGITAL SYSTEMS & DEVICE SIMULAION

FPGA (C-1)

[86] Jai Gopal Pandey, Abhijit Karmakar, Chandra Shekhar and S. Gurunarayanan. A Novel Architecture for FPGA Implementation of Otsu's Global Automatic Image Thresholding Algorithm

[294] Sharat Chandra Varma Bogaraju, Kolin Paul and M Balakrishnan. Accelerating Genome Assembly using Hard Embedded Blocks in FPGAs

[480] Burhan Mallik and Roohie Naaz Mir. A Hardware Intensive Approach for Efficient Implementation of Numerical Integration for FPGA Platforms

[49] Amin Ghasemazar, Mehran Goli and Ali Afzali-Kusha. Embedded Complex Floating Point Hardware Accelerator

LOW POWER DESIGN (C-2)

[71] Arnab Raha, Hrishikesh Jayakumar and Vijay Raghunathan. A Power Efficient Video Encoding Architecture using Re-configurable Approximate Circuits

[72] Hrishikesh Jayakumar, Arnab Raha and Vijay Raghunathan. QUICKRECALL: A Low Overhead HW/SW Approach for Enabling Computations across Power Cycles in Transiently Powered Computers

[53] Parastoo Kamranfar, Ali Shahabi, Ghazaleh Vazhbakht and Zain Navabi. Configurable Systolic Matrix Multiplication

[590] Neel Gala, Devanathan V.R., Karthik Srinivasan, V. Visvanathan and Kamakoti Veezhinathan. ProCA: Progressive Configuration Aware Design Methodology for Low Power Stochastic ASICs

DIGITAL DESIGN (C-3)

[281] Anand Darji, Saurabh Shukla, Shabbir Merchant and Arun Chandorkar. Hardware Efficient VLSI Architecture for 3-D Discrete Wavelet Transform

[315] Narayan Sugur, Saroja Siddamal and Samba Sivam Vemala. Design and Implementation of High Throughput and Area Efficient Hard Decision Viterbi Decoder in 65nm Technology

[428] Sundarrajan Rangachari, Jaiganesh Balakrishnan and Nitin Chandrachoodan. Scalable low power FFT/IFFT architecture with dynamic bit width configurability

[270] Santhosh Varma, Syed Ahmed and Srinivas M.B. A Decimal / Binary Multioperand Adder using a Fast Binary to Decimal Converter

PHYSICAL DESIGN (C-4)

[51] Bapi Kar, Susmita Sur-Kolay and C Mandal. Global Routing using Monotone Staircases with Minimal Bends

[167] Xing Wei, Tak-Kei Lam, Xiaoqing Yang, Wai-Chung Tang, Yi Diao and Yu-Liang Wu. Delete and Correct (DaC): an atomic logic operation for removing any unwanted wire

[253] Raghavan Kumar, Siva Nishok Dhanuskodi and Sandip Kundu. On Manufacturing-Aware Physical Design to Improve Uniqueness of Silicon-Based Physically Unclonable Functions

[50] Partha Pratim Saha and Tuhina Samanta. Obstacle Avoiding Rectilinear Clock Tree Construction with Skew Minimization

[172] Matthias Beste, Saman Kiamehr and Mehdi Tahoori. Layout–aware Delay Variation Optimization for CNTFET–based Circuits

MODELING & SIMULATION (C-5)

[150] Ayan Paul, Chaitanya Kshirsagar, Sachin Sapatnekar, Steven Koester and Chris Kim. Leakage Modeling for Devices with Steep Sub-threshold Slope Considering Random Threshold Variations

[173] Neha Sharan and Santanu Mahapatra. Small signal Non Quasi-static model for Common Double Gate MOSFET adapted to gate oxide thickness asymmetry.

[382] Parmanand Singh, Vivek Asthana, Anand Bulusu and Sudeb Dasgupta. Analytical Modeling of Sub-onset Current of Tunnel Field Effect Transistor

[444] Michael Meixner and Tobias Noll. Statistical modeling of glitching effects in estimation of dynamic power consumption

MODELING & ANALYSIS (C-6)

[478] Anupam Dutta, Saurabh Sirohi, Tamilmani Ethirajan, Harshit Agarwal, Yogesh Chauhan and Richard Williams. BSIM6 -Benchmarking the Next-Generation MOSFET Model For RF Applications

[557] Amrita Kumari and Subindu Kumar. Analysis of Nanoscale Strained-Si/SiGe MOSFETs including Source/Drain Series Resistance through a Multi-Iterative Technique

[574] Manodipan Sahoo, Prasun Ghosal and Hafizur Rahaman. An ABCD Parameter Based Modeling and Analysis of Crosstalk Induced Effects in Multiwalled Carbon Nanotube Bundle Interconnects

[405] Mukta Singh Parihar and Abhinav Kranti. Performance Optimization and Parameter Sensitivity Analysis of Ultra Low Power Junctionless MOSFETs

Track D: ANALOG/RF CIRCUITS & EMERGING TECHOLOGY

RF CIRCUITS (D-1)

[438] Rajesh Cheeranthodi, Santhosh Madhavan, Umesh K Shukla and Giri N Rangan. Improvements To Negative-C Compensation Based Amplifiers for Broadband Applications

[265] Sushrant Monga and Shouribrata Chatterjee. An Inductorless Continuous Time Feedback Equalizer with adapdtability for Gigabit Links in 0.13um CMOS

[508] Sivaramakrishna R and Shalabh Gupta. On dependence of amplitude noise versus offset frequency in LC oscillators

[385] Pradeep Karamcheti, Arunkumar Salimath and Achintya Halder. A 1 V, sub-mW, CMOS LNA for Low-power 1-GHz Wide-band Wireless Applications

LP-CIRCUITS (D-2)

[92] Sanjay Wadhwa, Jaideep Banerjee and Rakesh Gupta. Low Power Single Amplifier Voltage Regulator

[298] Matthew Morrison and Nagarajan Ranganathan. Forward Body Biased Adiabatic Logic for Peak and Average Power Reduction in 22nm CMOS

[74] Sourindra Chaudhuri and Niraj Jha. FinFET Logic Circuit Optimization with Different FinFET Styles: Lower Power Possible at Higher Supply Voltage

[426] Lokesh Siddhu, Amit Mishra and Virendra Singh. Operand Isolation circuits with reduced overhead for Low power Data-path design

[568] Mohammad Yousef Zarei and Siamak Mohammadi. High-speed, Low-Power Quasi Delay Insensitive handshake circuits based on FinFET Technology

MEMS/Bio Chips (D-3)

[66] Pramod Kaddi, Basireddy Karunakar Reddy and Shiv Govind Singh. Active Cooling Technique for Efficient Heat Mitigation in 3D-ICs

[162] Prasad Avss, Venkatesh Kp, Rudra Pratap and Navakanta Bhat. Improved design methodology for the development of electrically actuated MEMS structures

[200] Sukanta Bhattacharjee, Ansuman Banerjee, Krishnendu Chakrabarty and Bhargab Bhattacharya. Correctness Checking of Bio-chemical Protocol Realizations on a Digital Microfluidic Biochip

[504] Pranab Roy, Samadrita Bhattacharyya, Rupam Bhattacharya, Hafizur Rahaman and Parthasarathi Dasgupta. A novel wire planning technique for optimum pin utilization in Digital Microfluidic Biochips

ANALOG CIRCUITS – 1 (D-4)

[331] Saurabh Singh and Nitin Bansal. Output impedance as figure of merit to predict transient performance for embedded linear voltage regulators

[402] Karthik Ramkumar Jeyashankar, Makrand Mahalley and Bharadwaj Amrutur. A Time-based Low Voltage Body Temperature Monitoring Unit

[473] Vinayak Gopal Hande and Maryam Shojaei Baghini. Trimless, PVT Insensitive Voltage Reference using Compensation of Beta and Thermal Voltage

[475] Bhuvanan K and Vijaya Sankara Rao P. A Low Power CMOS Imager Based on Distributed Compressed Sensing

EMERGING TECHNOLOGIES (D-5)

[328] Kamalika Datta and Indranil Sengupta. All Optical Reversible Multiplexer Design using Mach-Zehnder Interferometer

[468] Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan. Circuit for Reversible Quantum Multiplier Based on Binary Tree Optimizing Ancilla and Garbage Bits

[553] Jayashree Hv, Himanshu Thapliyal and Vinodkumar Agrawal. Design of Dedicated Reversible Quantum Circuitry for Square Computation

[569] Sai Phaneendra P, Chetan Vudadha, Sreehari Veeramachaneni and Srinivas Mb. An Optimized Design of Reversible Quantum Comparator

ANALOG CIRCUITS -2 (D-6)

[434] Metilda Sagaya Mary N.J, Ashis Maity and Amit Patra. Light Load Efficiency Improvement in High Frequency DC-DC Buck Converter using Dynamic Width Segmentation of Power MOSFETs

[448] Chithira Ravi, Rahul Thottathil and Bibhudatta Sahoo. Histogram Based Deterministic Digital Background Calibration for Pipelined ADCs

[470] Gopikrishnan Radhakrishnan, Vijaya Sankara Rao Pasupureddi and Govindarajulu Regeti. A Power Efficient Fully Differential Back Terminated Current-Mode HDMI Source

[506] Makarand Shirasgaonkar, Roxanne Vu, Deborah Dressler, Nhat Nguyen, Kambiz Kaviani and Yueyong Wang. An Adaptive Body-Biased Clock Generation System in 28nm CMOS